ANNA UNIVERSITY COIMBATORE

B.E./B.TECH. DEGREE EXAMINATIONS: MAY/JUNE 2010

REGULATIONS: 2008

FOURTH SEMESTER: INFORMATION TECHNOLOGY

080250011-COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 3 Hours **Max.Marks:100**

PART-A

(20*2=40 Marks)

ANSWER ALL QUESTIONS

1. Mention the registers used for communication between processor and man memory.
2. Compare CSIC and RISC with respect to complexity.
3. Give an example on Index addressing mode.
4. What is meant by straight line sequencing?
5. How to transfer the contents of register R1 register R4.
6. Write the features of multiple bus organization.
7. Write a micro routine for executing the instruction on negative.
8. Write any two advantages of using Nano programming?
9. Mention the data hazards that occur during pipeline operation.
10. What role the Cache memory can perform in pipeline implementation.
11. What are the factors considered for deciding the number of pipeline stages in a system?
12. What is the meant by memory interleaving?
13. How read and write operation is performed in static memory.
14. Differentiate write-through and write-back update methods in cache memory.
15. Write the function of translation look a side buffer.
16. How to handle miss penalties in a memory subsystem.
17. What is the difference between a subroutine and interrupt service routine?
18. Sate the importance of DMA in networks.
19. Write the function of bus arbiter in DMA interface.

20. What are the advantages of using USB based devices.

PART-B

(5*12=60 Marks)

ANSWER ANY FIVE QUESTIONS

21. Register R5 in a program is used to point to the top of stack. Write a sequence of instruction using indexed, auto increment and auto decrement addressing modes to perform each of the following tasks: (12)

i) Pop the top two items off the stack, add them, and then push the result on to attack.

ii) Copy the fifth item from the top into register R3.

iii) Remove the top ten items from the stack.

22. Write note on: micro program sequencing and wide branch addressing. (12)

23 (a). Discuss the influence of pipelining in designing the instruction set with an example (6)

(b). Explain the data dependency concept in pipelining environment. (6)

24 (a). Explain the address translation mechanism of virtual memory with suitable diagram (6)

(b) Explain the features and characteristics of semiconductor RAM memory. (6)

25 (a). A block-set-associative cache consists of a total of 64 blocks divided into four block sets. The main memory contains 4096 blocks, each consisting of 128 words (8)

(i) How many bits are there in a main memory address?

(ii) How many bits are there in each of the TAG, SET and WORD fields?

b) Discuss the limitations on associative memories. (4)

26 (a). Discuss the features and function of SCSI bus. (8)

(b) Illustrate the handshake control of data transfer in asynchronous bus (4)

27. Explain the bus arbitration mechanism in DMA interface. (12)

28. Discuss the exception handling mechanisms when pipelining is implemented in the system. Trace using a suitable example. (12)

**********THE END**********