Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 10277

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2012.

Sixth Semester

Computer Science and Engineering

CS 2354/CS 64/10144 CS 604 — ADVANCED COMPUTER ARCHITECTURE

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Define Instruction level parallelism.

2. What are the advantages of using dynamic scheduling?

3. What are the advantages and disadvantages of trace scheduling method?

4. What are the limits on Instruction Level Parallelism?

5. What is Multiprocessor Cache Coherence?

6. Distinguish between fine-grained and coarse-grained multithreading.

7. Why do DRAMs generally have much larger capacities than SRAMs constructed in the same fabrication technology?

8. What is the average time to read or write a 512-byte sector for a disk? The advertised average seek time is 5 ms. the transfer rate is 40 MB/second, it rotates at 10000 RPM, and the controller overhead is 0.1 ms. Assume the disk is idle so that there is no queuing delay.

9. What is Multi-Core Architectures?

10. What are the advantages of CMP architecture?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain in details about the various dependences caused in ILP. (8)

(ii) Explain the static and dynamic branch prediction schemes in detail. (8)

Or

(b) (i) Explain the Tomasulo's Approach used in dynamic scheduling for overcoming data hazards. (8)

(ii) Describe how the compiler technology can be used to improve the performance of instruction level parallelism. (8)

12. (a) (i) Explain the software pipelining method used for uncover parallelisim. (8)

(ii) Compare the Hardware speculation with software speculation. (8)

Or

(b) Discuss the essential features of Intel IA-64 Architecture and Itanium Processor. (16)

13. (a) (i) Discuss the various cache-coherence protocols used in symmetric shared memory architecture. (8)

(ii) What are the hardware primitives available to resolve synchronization issues in a multi-processor environment? Give examples. (8)

Or

(b) (i) Discuss the performance of Symmetric Shared-Memory Multiprocessors for a multi-programmed workload consisting of both user activity and OS activity. (8)

(ii) Discuss the various memory consistency models. (8)

14. (a) (i) Discuss the various techniques available for reducing cache miss penalty. (8)

(ii) Briefly discuss the various levels of RAID. (8)

Or

(b) (i) Write short notes on Compiler Optimizations to reduce the miss rate. (8)

(ii) Explain the steps involved in the designing of an I/O system. (8)

15. (a) (i) Explain in detail about SMT architecture and its challenges (8)

(ii) Discuss in detail about heterogeneous multi-core processors. (8)

Or

(b) (i) Explain the CMP architecture in detail. (8)

(ii) Explain the IBM cell processor concept in detail. (8)
